

FIG. 1

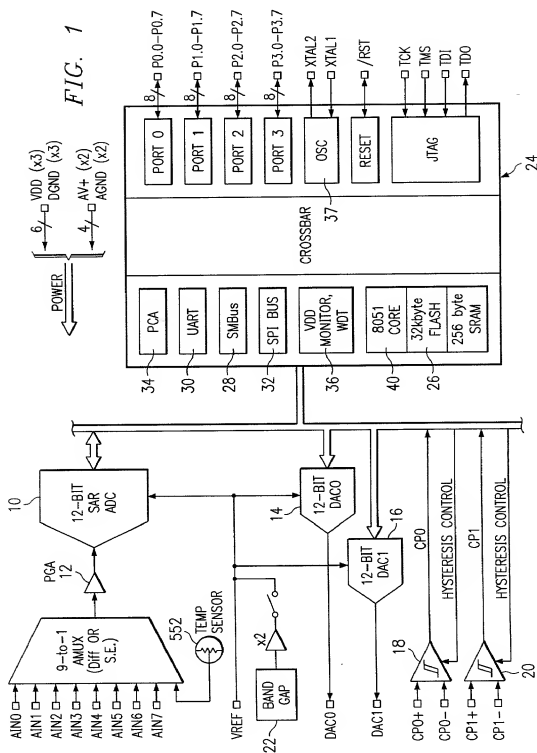


FIG. 2

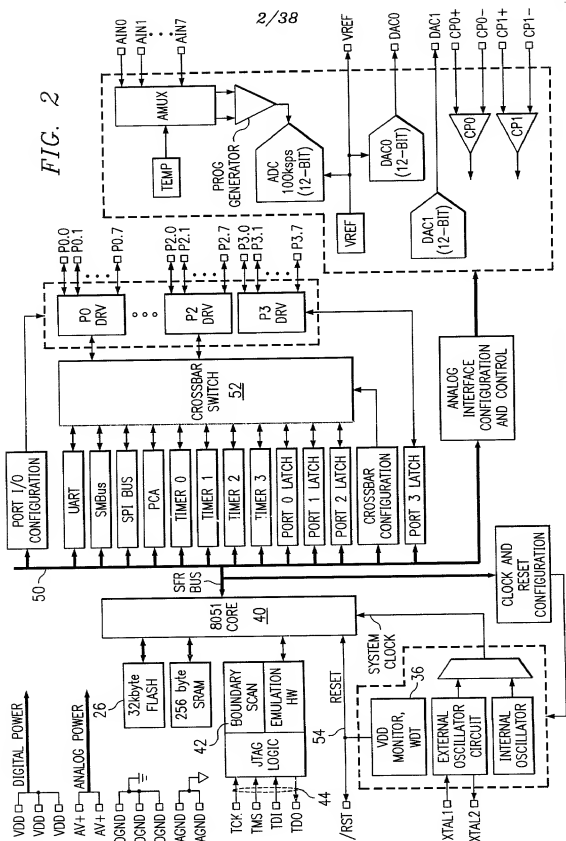
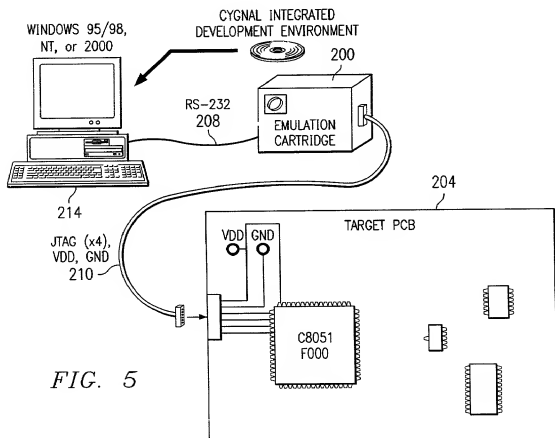
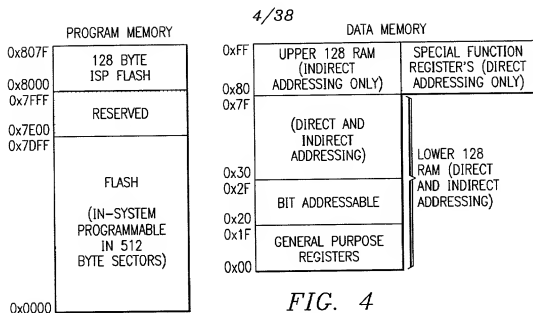


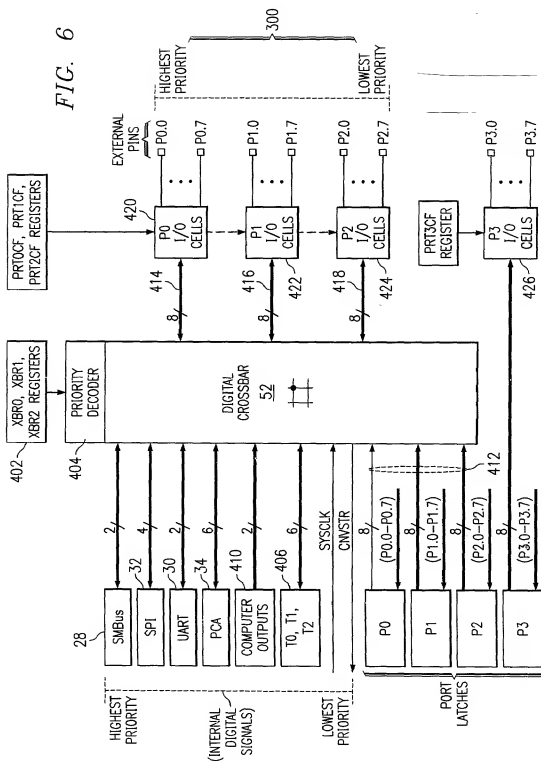


FIG. 3



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FIG. 6



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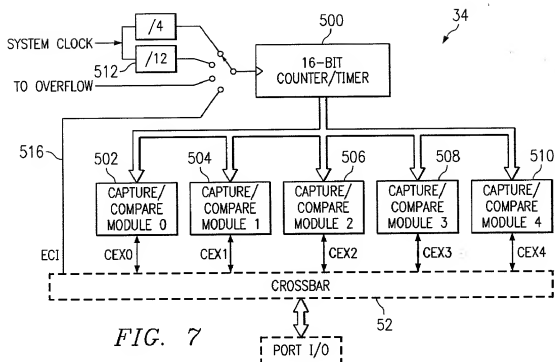


FIG. 7

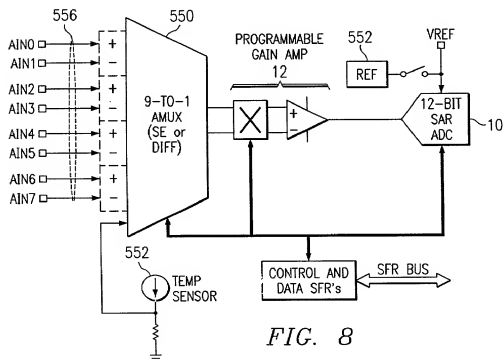
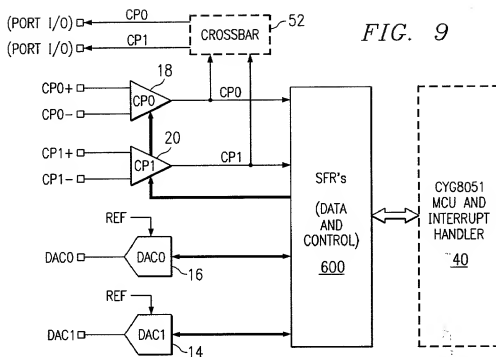
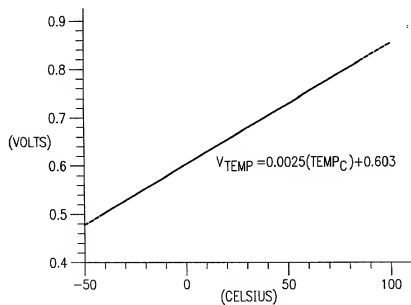


FIG. 8

**FIG. 12**

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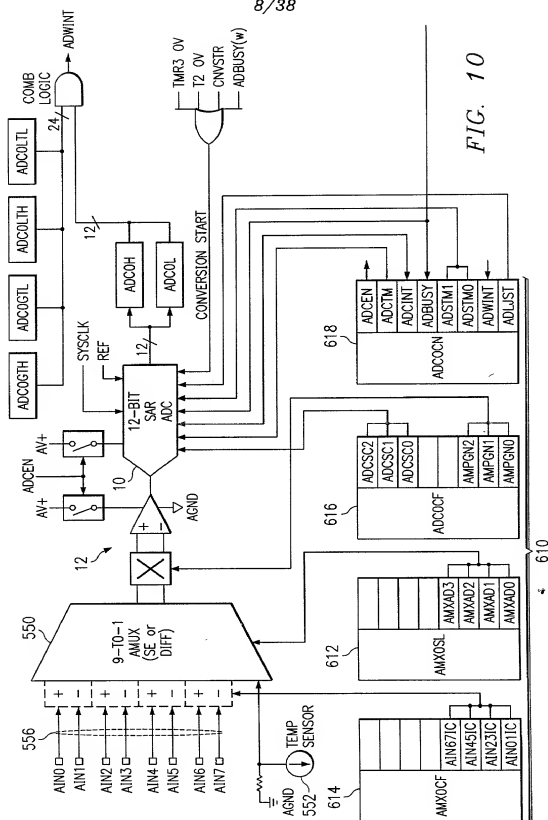


FIG. 10

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FIG. 11A

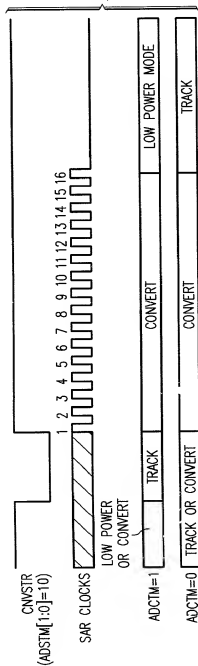
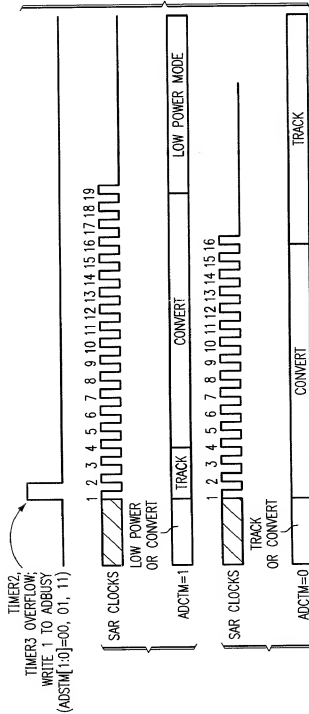


FIG. 11B



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INPUT VOLTAGE (A00-AGND)	ADC DATA WORD	INPUT VOLTAGE (A00-AGND)	ADC DATA WORD
REF x (4095/4096)	0x00FF	REF x (4095/4096)	0x00FF
	0x0201		0x0201
	0x0200		0x0200
REF x (512/4096)	0x01FF	REF x (512/4096)	0x01FF
	0x0101		0x0101
	0x0100		0x0100
REF x (256/4096)	0x00FF	REF x (256/4096)	0x00FF
	0x0000		0x0000

GIVEN:

AMX0SL=0x00, AMX0CF=0x00, ADJUST=0,
 ADC0LTH+ADC0LTL=0x0200,
 ADC0GTH+ADC0GTL=0x0100.

AN ADC END OF CONVERSION WILL CAUSE AN ADC WINDOW
 COMPARE INTERRUPT (ADWINT=1) IF THE RESULTING ADC
 DATA WORD IS < 0x0200 AND > 0x0100.

GIVEN:

AMX0SL=0x00, AMX0CF=0x00, ADJUST=0,
 ADC0LTH+ADC0LTL=0x0100,
 ADC0GTH+ADC0GTL=0x0200.

AN ADC END OF CONVERSION WILL CAUSE AN ADC WINDOW
 COMPARE INTERRUPT (ADWINT=1) IF THE RESULTING ADC
 DATA WORD IS < 0x0100 OR > 0x0200.

TO FIG. 13B

FIG. 13A

FIG. 13B

FROM FIG. 13A

INPUT VOLTAGE (AD0-AD1)	ADC DATA WORD	INPUT VOLTAGE (AD0-AD1)	ADC DATA WORD
REF x (4095/4096)	0x07FF	REF x (4095/4096)	0x07FF
	0x0101		0x0101
REF x (256/4096)	0x0100	REF x (256/4096)	0x0100
	0x00FF		0x00FF
	0x0000		0x0000
REF x (-1/4096)	0xFFFF	REF x (-1/4096)	0xFFFF
	0xFFFE		0xFFFE
-REF	0xF800	-REF	0xF800

ADWINT
NOT AFFECTED

ADCOLTH-ADCOLTL

ADWINT=1

ADCOLTH-ADCOLTL

ADWINT
NOT AFFECTED

ADWINT=1

ADCOLTH-ADCOLTL

ADWINT
NOT AFFECTED

ADCOLTH-ADCOLTL

ADWINT=1

GIVEN:

AMX0SL=0x00, AMX0CF=0x01, ADJUST=0,
ADCOLTH-ADCOLTL=0x0100,
ADCOLGTH-ADCOLGTL=0xFFFF.

AN ADC END OF CONVERSION WILL CAUSE AN ADC WINDOW
COMPARE INTERRUPT (ADWINT=1) IF THE RESULTING ADC
DATA WORD IS < 0x0100 AND > 0xFFFF. (TWO'S
COMPLEMENT MATH.)

GIVEN:

AMX0SL=0x00, AMX0CF=0x01, ADJUST=0,
ADCOLTH-ADCOLTL=0xFFFF,
ADCOLGTH-ADCOLGTL=0x0100.

AN ADC END OF CONVERSION WILL CAUSE AN ADC WINDOW
COMPARE INTERRUPT (ADWINT=1) IF THE RESULTING ADC
DATA WORD IS < 0xFFFF OR > 0x0100. (TWO'S COMPLEMENT
MATH.)

INPUT VOLTAGE (ADD-AGND)	ADC DATA WORD	INPUT VOLTAGE (ADD-AGND)	ADC DATA WORD
REF x (4095/4096)	0xFF0	REF x (4095/4096)	0xFF0
	0x2010		0x2010
REF x (512/4096)	0x2000	REF x (512/4096)	0x2000
	0x1FF0		0x1FF0
	0x1010		0x1010
REF x (256/4096)	0x1000	REF x (256/4096)	0x1000
	0x0FF0		0x0FF0
0	0x0000	0	0x0000

GIVEN:

AMXOSL=0x00, AMXOCF=0x00, ADJUST=1,
ADCOLTHADCOLTL=0x2000,
ADCOGTHADCOGTL=0x1000.

AN ADC END OF CONVERSION WILL CAUSE AN ADC WINDOW
COMPARE INTERRUPT (ADWINT=1) IF THE RESULTING ADC
DATA WORD IS < 0x2000 AND > 0x1000.

GIVEN:

AMXOSL=0x00, AMXOCF=0x00, ADJUST=1,
ADCOLTHADCOLTL=0x1000,
ADCOGTHADCOGTL=0x2000.

AN ADC END OF CONVERSION WILL CAUSE AN ADC WINDOW
COMPARE INTERRUPT (ADWINT=1) IF THE RESULTING ADC
DATA WORD IS < 0x1000 OR > 0x2000.

TO FIG. 14B

FIG. 14A

FIG. 14B

FROM FIG. 14A

INPUT VOLTAGE (AD0-AD1)	ADC DATA WORD	INPUT VOLTAGE (AD0-AD1)	ADC DATA WORD
REF x (4095/4096)	0x7FF0	REF x (4095/4096)	0x7FF0
	ADWINT NOT AFFECTED		ADWINT=1
REF x (256/4096)	0x1010		0x1010
REF x (256/4096)	0x1000	REF x (256/4096)	0x1000
	ADWINT NOT AFFECTED		ADWINT NOT AFFECTED
REF x (-1/4096)	0xFFFO	REF x (-1/4096)	0xFFFO
	ADWINT NOT AFFECTED		ADWINT=1
-REF	0x8000	-REF	0x8000

GIVEN:

AMXOSL=0x00, AMXOCF=0x01, ADJUST=1,
ADCOLTH+ADCOLTL=0x1000,
ADCOGTH+ADCOGTL=0xFFFO.

AN ADC END OF CONVERSION WILL CAUSE AN ADC WINDOW
COMPARE INTERRUPT (ADWINT=1) IF THE RESULTING ADC
DATA WORD IS < 0x1000 AND > 0xFFFO. (TWO'S
COMPLEMENT MATH.)

GIVEN:

AMXOSL=0x00, AMXOCF=0x01, ADJUST=1,
ADCOLTH+ADCOLTL=0xFFFO,
ADCOGTH+ADCOGTL=0x1000.

AN ADC END OF CONVERSION WILL CAUSE AN ADC WINDOW
COMPARE INTERRUPT (ADWINT=1) IF THE RESULTING ADC
DATA WORD IS < 0xFFFO OR > 0x1000. (TWO'S COMPLEMENT
MATH.)

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FIG. 15

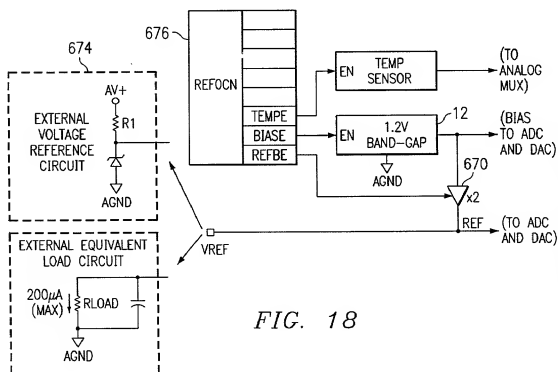
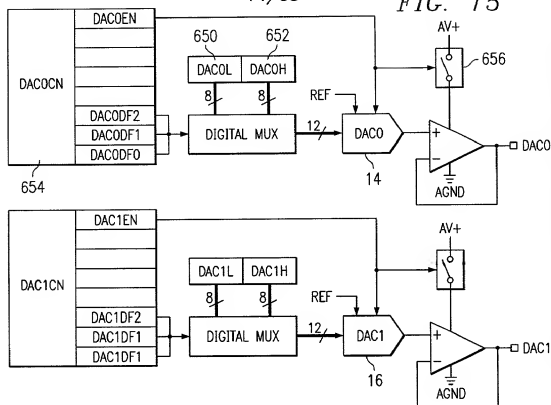


FIG. 18

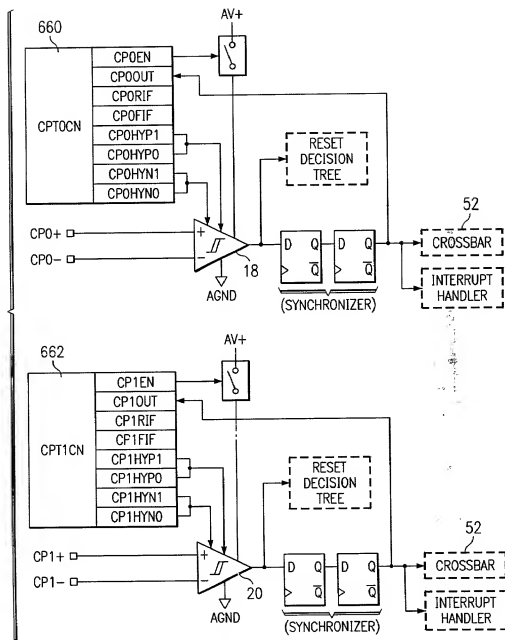


FIG. 16

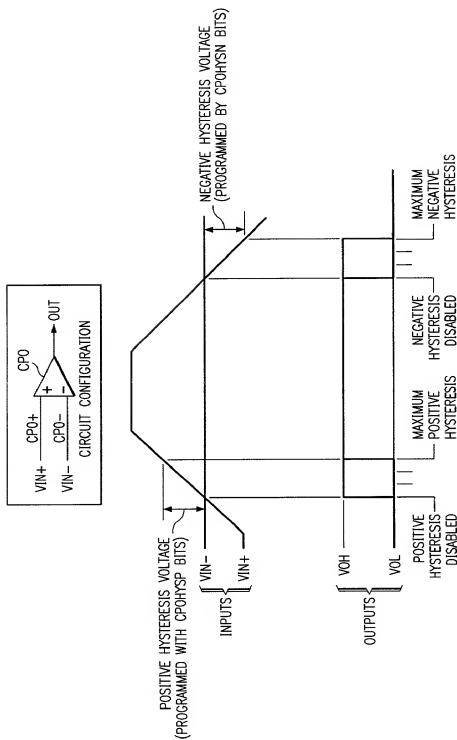
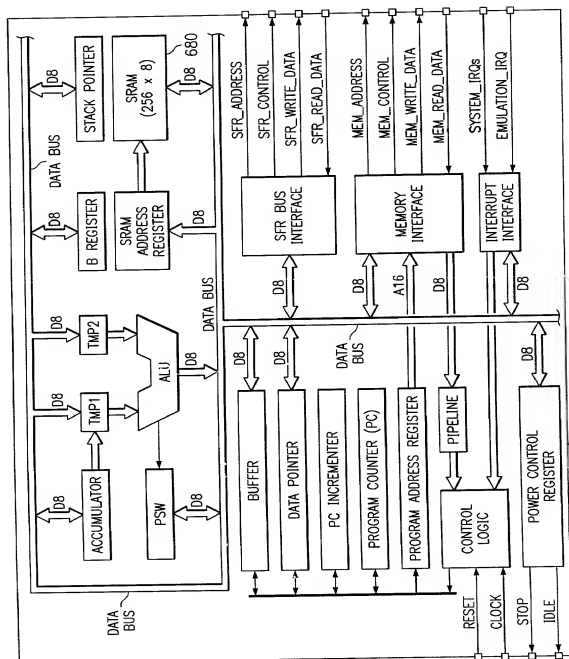


FIG. 17

FIG. 19



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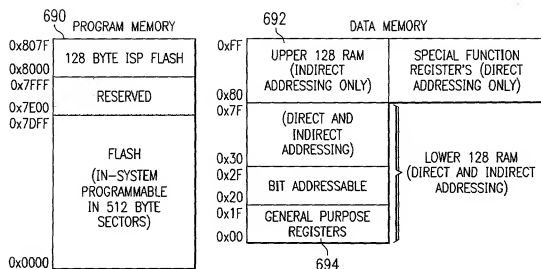


FIG. 20

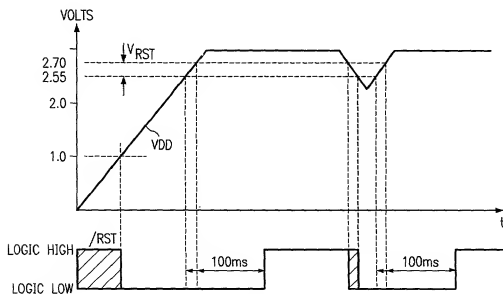
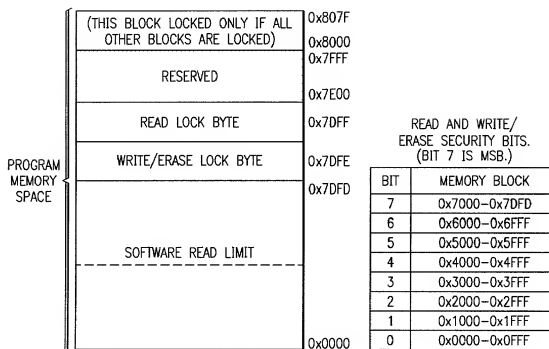


FIG. 22

**FLASH READ LOCK BYTE**

BITS 7-0: EACH BIT LOCKS A CORRESPONDING BLOCK OF MEMORY. (BIT 7 IS MSB.)

0: READ OPERATIONS ARE LOCKED (DISABLED) FOR CORRESPONDING BLOCK ACROSS THE JTAG INTERFACE.

1: READ OPERATIONS ARE UNLOCKED (ENABLED) FOR CORRESPONDING BLOCK ACROSS THE JTAG INTERFACE.

FLASH WRITE/ERASE LOCK BYTE

BITS 7-0: EACH BIT LOCKS A CORRESPONDING BLOCK OF MEMORY.

0: WRITE/ERASE OPERATIONS ARE LOCKED (DISABLED) FOR CORRESPONDING BLOCK ACROSS THE JTAG INTERFACE.

1: WRITE/ERASE OPERATIONS ARE UNLOCKED (ENABLED) FOR CORRESPONDING BLOCK ACROSS THE JTAG INTERFACE.

FLASH ACCESS LIMIT REGISTER (FLACL)

THE CONTENT OF THIS REGISTER IS USED AS THE HIGH BYTE OF THE 16-BIT SOFTWARE READ LIMIT ADDRESS. THE 16-BIT READ LIMIT ADDRESS VALUE IS CALCULATED AS 0xNN00 WHERE NN IS REPLACED BY CONTENT OF THIS REGISTER ON RESET. SOFTWARE RUNNING AT OR ABOVE THIS ADDRESS IS PROHIBITED FROM USING THE MOVX AND MOVC INSTRUCTIONS TO READ, WRITE, OR ERASE, LOCATIONS BELOW THIS ADDRESS. ANY ATTEMPTS TO READ LOCATIONS BELOW THIS LIMIT WILL RETURN THE VALUE 0x00.

FIG. 21

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FIG. 23

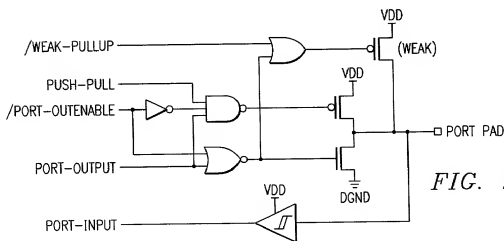
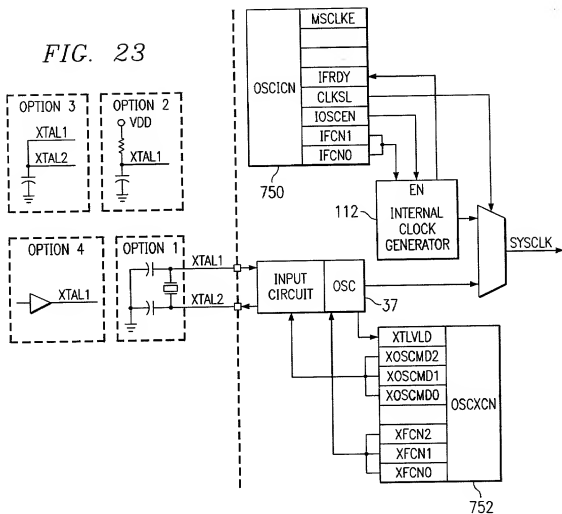


FIG. 24

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FIG. 25A

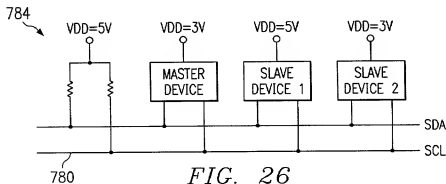
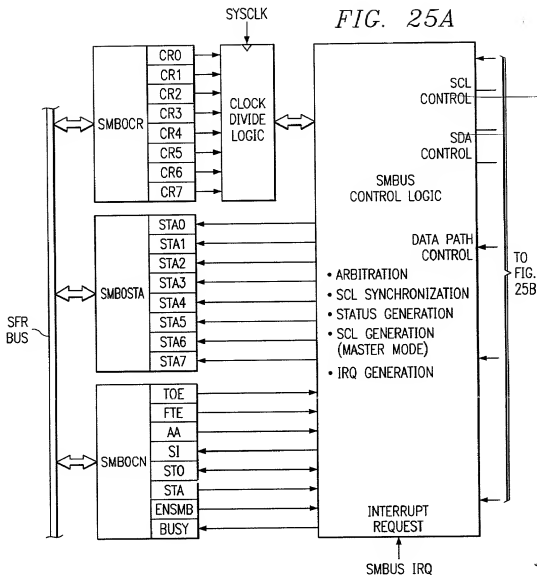
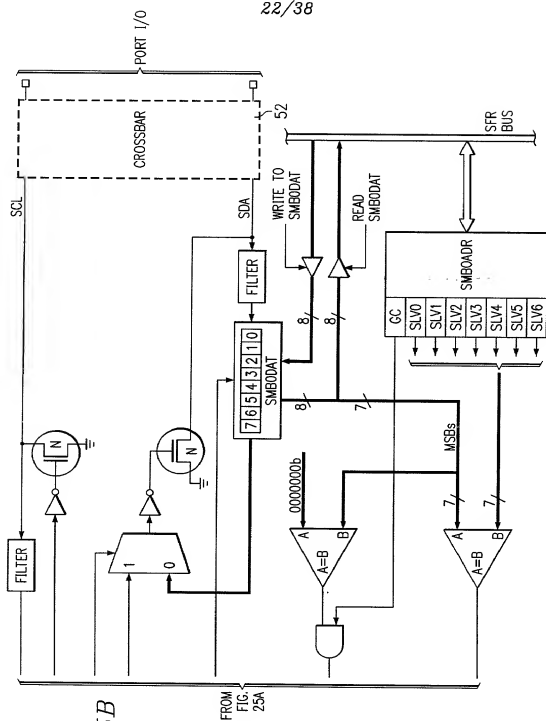
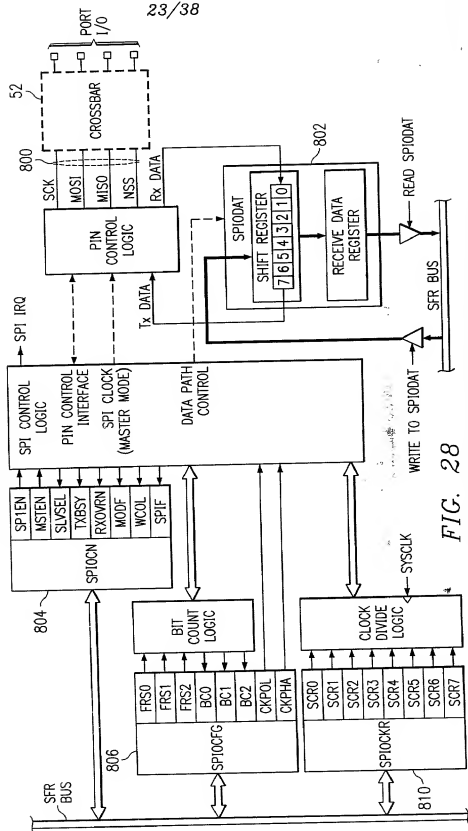
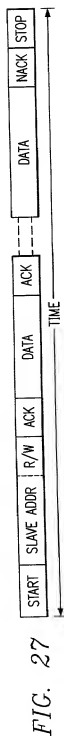


FIG. 26





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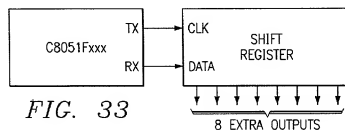
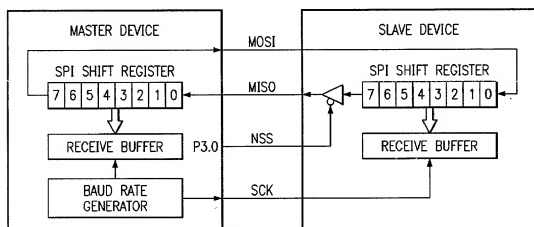
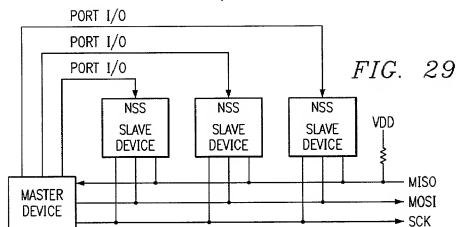


FIG. 31

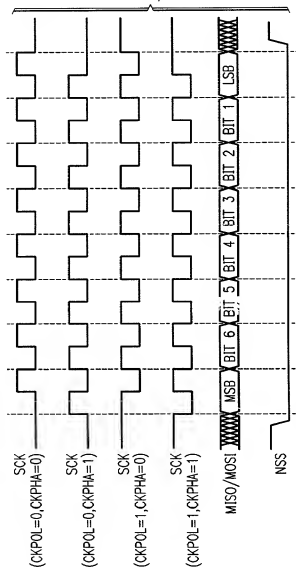


FIG. 34

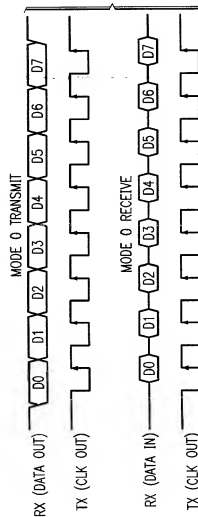
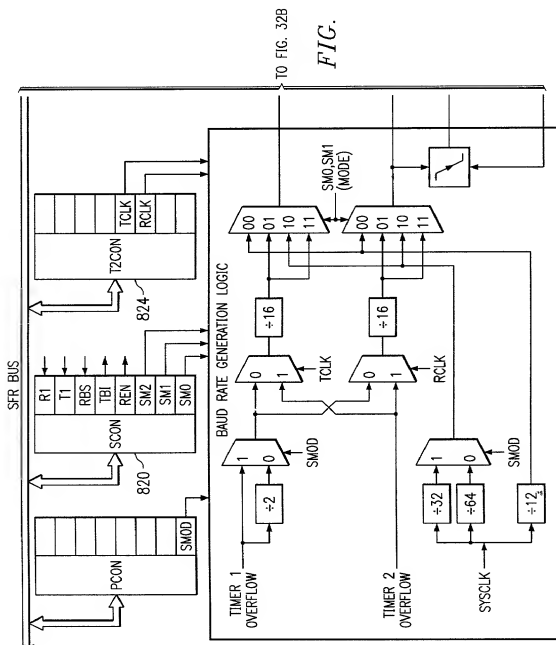
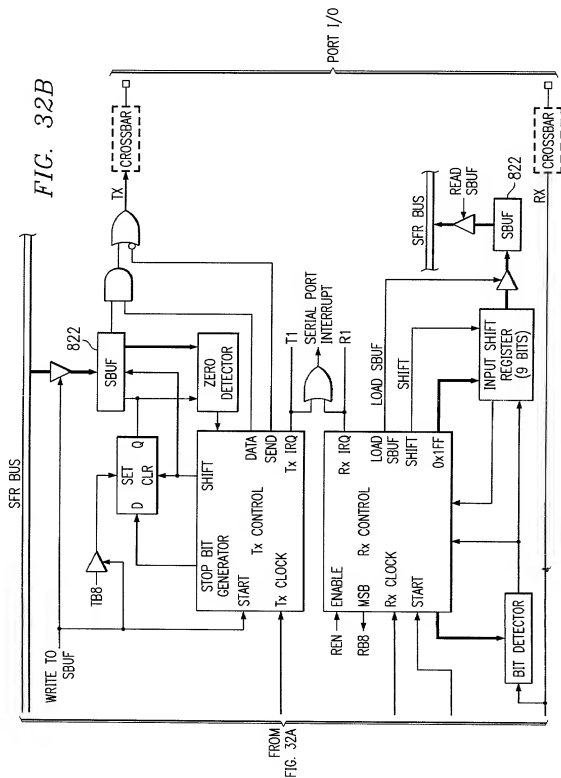


FIG. 32A



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FIG. 32B



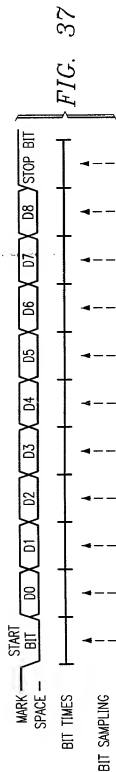
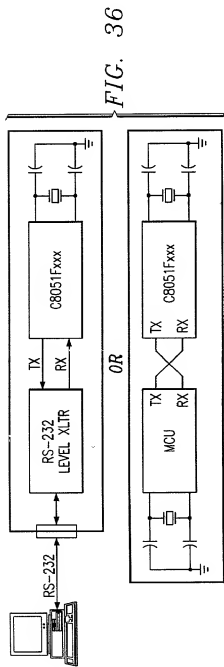
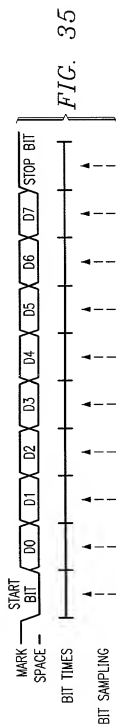


FIG. 38

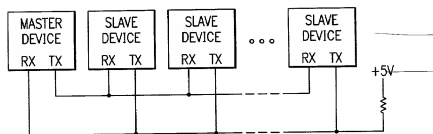
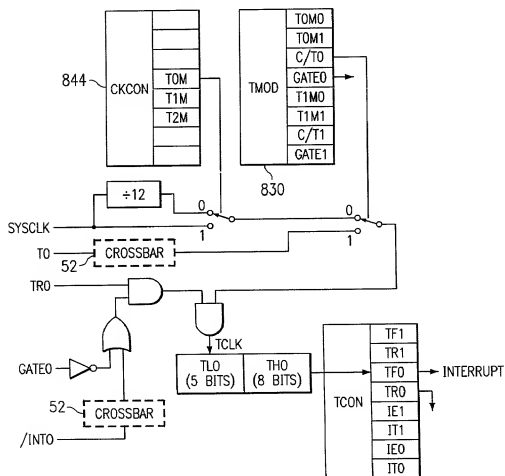


FIG. 39



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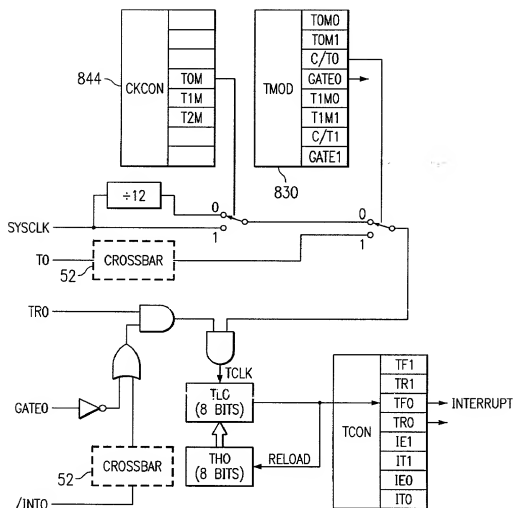


FIG. 40

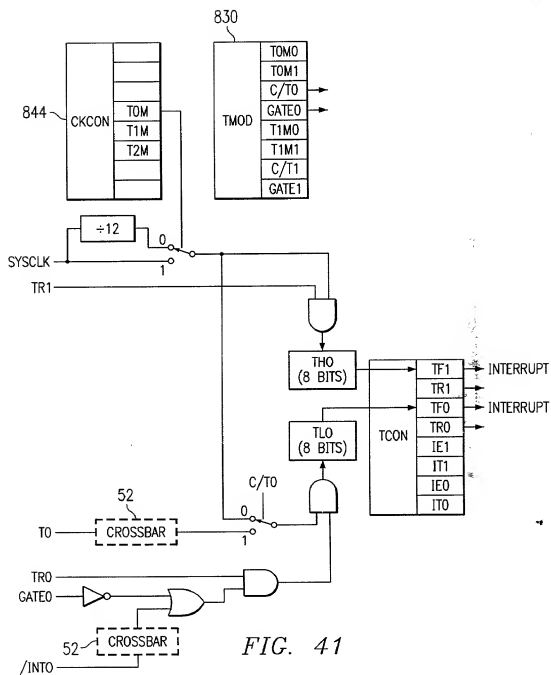


FIG. 42

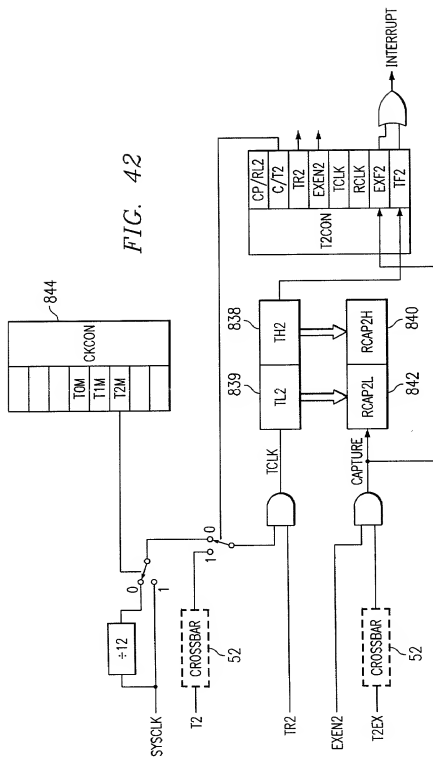
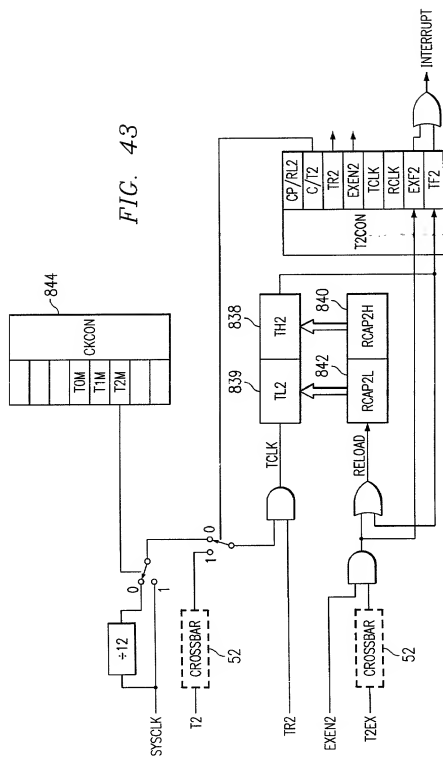


FIG. 43



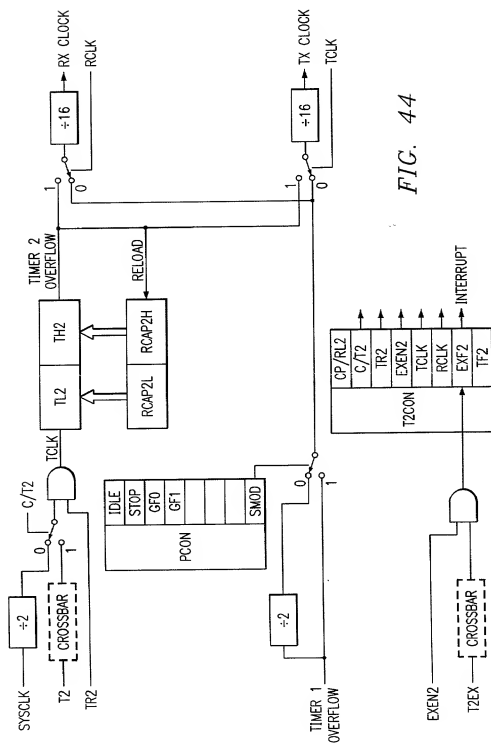


FIG. 44

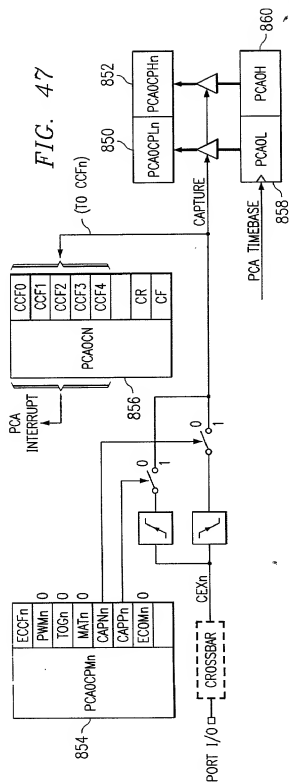
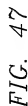


FIG. 46

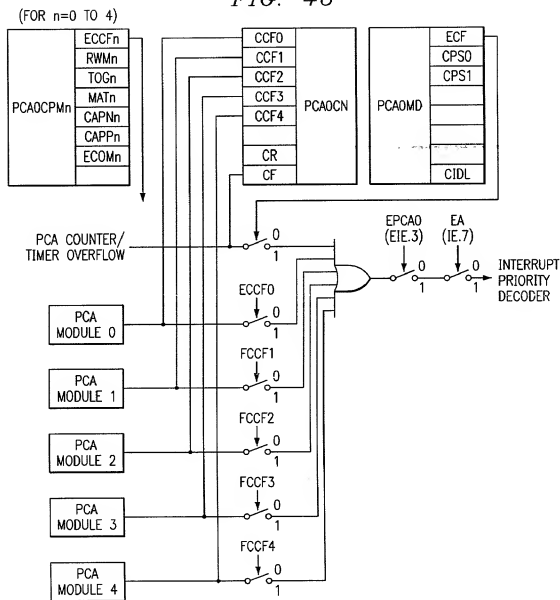


FIG. 48

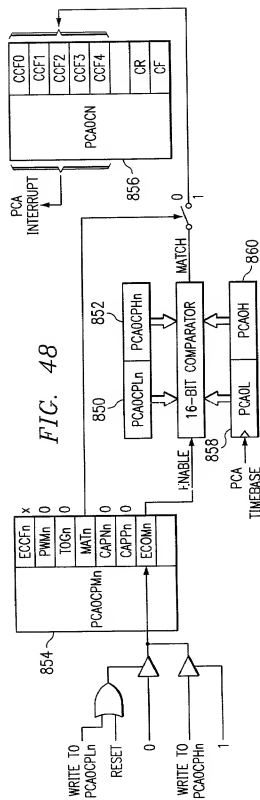
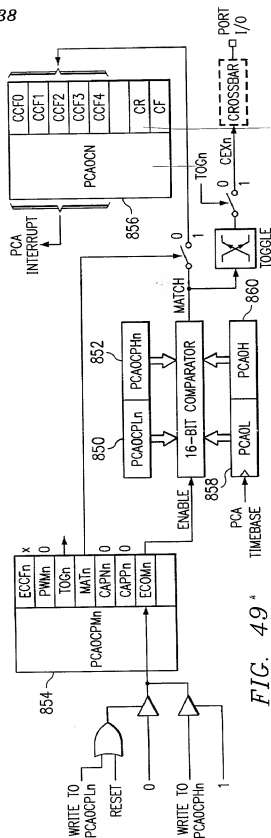


FIG. 49 *



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